A DELAY LOCK LOOP CIRCUIT USEFUL IN A SYNCHRONOUS SYSTEM AND ASSOCIATED METHODS

Abstract

A method and circuitry for a delay lock loop useful in synchronizing the accessing of a memory array with a system clock is disclosed. In a preferred embodiment, the delay lock loop includes a variable delay element. The delay of the variable delay element is initially set to a minimum delay value. The system clock is then frequency divided and sent to the variable delay element, the output of which will ultimately be used to access the memory array in a synchronized manner with the system clock. The frequency divided clock and the output of the variable delay element are input to a phase detector, which creates a control signal for adjusting the delay of the variable delay element. After the signals are determined to be locked by the phase detector, an undivided clock signal version of the clock signal is sent to the variable delay element, and a frequency divided version of the output of the variable delay element is sent to the phase detector in lieu of the previous output of the variable delay element.